DL501

TDC

Manual

PhIHD vwa
Test

DL501 Data Sheet : Digital to Time Converter

Frontpanel Signals

*	+5V/-5V	VME power
*	Sel	module was accessed
*	Busy	lit if sampling
*	Hit/Data	lit on first Hit/data in memory
<	Clock	NIM, ≤ 100 MHz
<	Start/Gat	NIM, (asynchron with clock!)
<	Stop/Trig	NIM, (Trig=ext.HitTrigger)
<	Reset	NIM, Fast Clear
>	Busy/Data	NIM,
>	Hit	NIM,
	-5V	Front Connector for -5V
	GND	if using std. VME crates!
	GND,GND	
>	+5V,-5V	< 500mA
<	±Ch17	diff ECL
<	±Ch16	diff ECL
<	±Ch15	diff ECL
<	±Ch0	diff ECL

Application

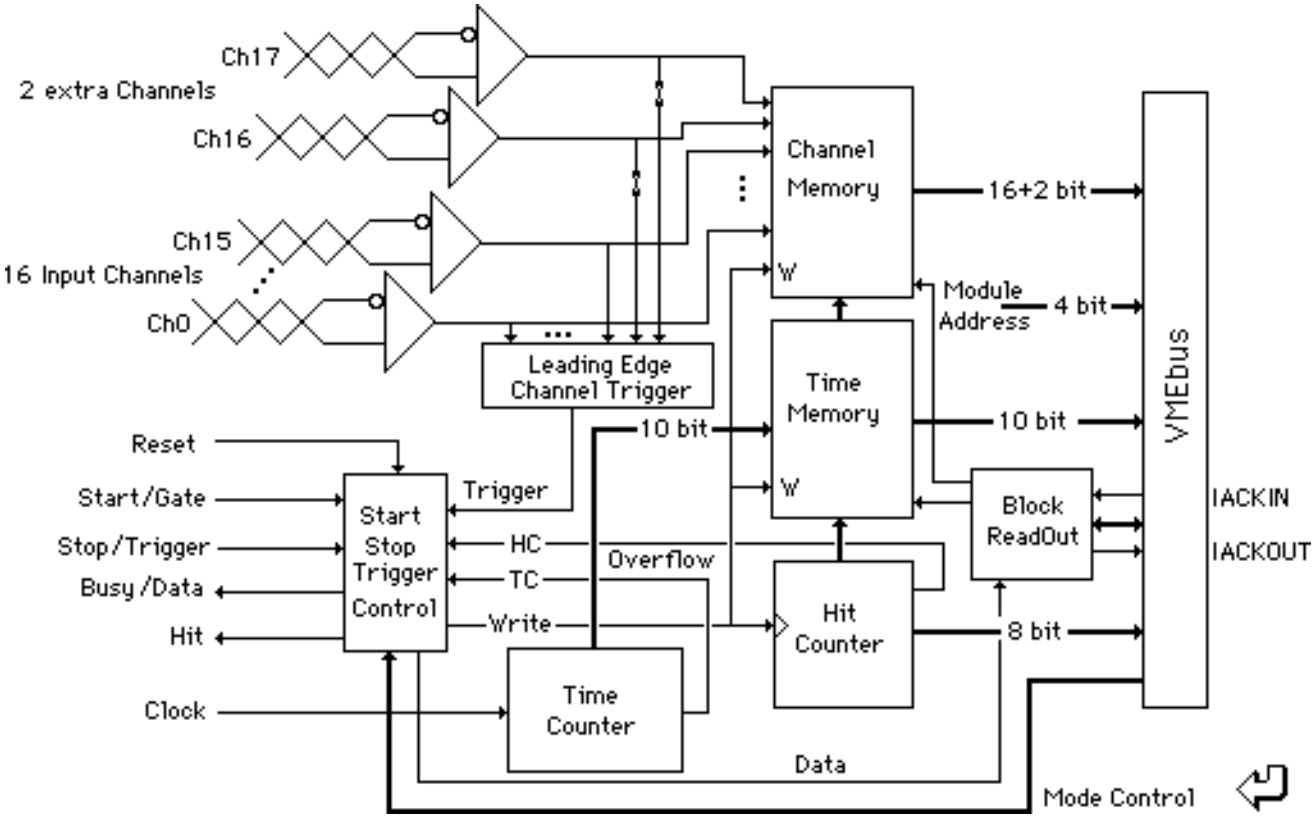
Multichannel Driftchambers
Input from DL504 Discriminator

Features

Number of channels: 16 + 2
Time Resolution: 1/F (F ≤ 100MHz)
Range:(256-HitSlices)*1024*1/F
= 2.68 ms (0 HitSlices, F=100MHz)
= 10 µs (255 HitSlices, F=100MHz)
Dead Time (one channel): 20 ns
Conversion & Time: digital, 0s
Storage: only valid data
Multi-Hits (one channel): ≤ 255
Multi-Events: ≤ 255
Trigger: leading edge on any channel, external
Start: software, external, on Gate (rising edge)
Stop: software, external, on Gate (falling edge)
on Timecounter (TC) overflow,
on Hitcounter (HC) overflow
FastClear: < 20 ns, software, external
Interrupt: first hit; Readout: Auto Blockmode
onboard Quartzclock

Package: VME-Double Eurocard (Size B), 4 TE width
Power: 5.3A @ -5.2V; .85A @ +5V;

DL501 Blockdiagram



DL501 Circuit Description

After RESET a START Signal (both either from software or external!) will start the recording of the times of leading edges of analog input signals. The time reference (10 Bits) is given by the TIME COUNTER (TC) which is also started and clocked from an external (or internal) CLOCK (F≤100MHz).

18 differential input CHANNELS are sampled with the clock and whenever the trigger logic detects a rising edge on one of the input signals it will generate a trigger signal. This trigger signal causes the writing of the current time to the TIME MEMORY and the writing of the current channel pattern to the CHANNEL MEMORY. The current channel pattern shows for all channels only those which are starting in this moment! 2 of the 18 channels can be configured (by jumpers) to record only the state at time of trigger. Any channel can be disabled individually by software.

After recording of the hit the HIT COUNTER is incremented by one and the circuit waits for the next hit!

On overflow of the TIME COUNTER a MARKER hit with this time (=1023) will be generated. If there is a real signal trigger at this moment the according channel pattern will also be recorded!

The memory is now filled according to the conditions described in 'DL501 Recording Modes'.
After stop the HitCounter can be read out to determine the number of valid hits in the TDC Memory!

In NON GATED MODE the stop, either by TC OVERRUN, HC OVERRUN or external STOP, will always be recorded as a last MARKER hit! Therefore the number of valid hits is here HITCOUNTER -1.
In GATED MODE the module simply stops on End Of Gate and no MARKER hit will be written.

Channel pattern (18 bits), Time information (10 bits) and module number (4 bits) is packed in one 32 bit word and has to be read out sequentially in the order last to first! A special block transfer mode enables fast readout of all modules and is terminated on empty with BUSERROR!

DL501 Recording Modes

The DL501 TDC can be operated in 4 Modes according to the combinations of two programmable STOP conditions (besides of stopping with external STOP/GATE or software Stop!):
- TC-STOP: Stop on TimeCounter overflow =1023
- HC-STOP: Stop on HitCounter overflow = 255 (when memory is completely filled!)

a) TC-STOP + HC-STOP: The TDC stops on either TimeCounter or HitCounter overflow.
This is the typical COMMON START mode where the first hits after start are essential.
-High signal rates: only the first 255 hits (after start) are valid!
-Low signal rates: all n<255 hits (before automatic stop on TC overflow) are valid!
-No signals: the memory is filled with only one (marker) hit!

b) TC-STOP + NOT HC-STOP: The TDC stops only on TimeCounter overrun.
This is also COMMON START mode where the last hits before automatic stop are essential.
-High signal rates: only the last 255 hits (before automatic stop on TC overrun) are valid!
-Low signal rates: all n<255 hits (before automatic stop on TC overflow) are valid!
-No signals: the memory is filled with only one (marker) hit!

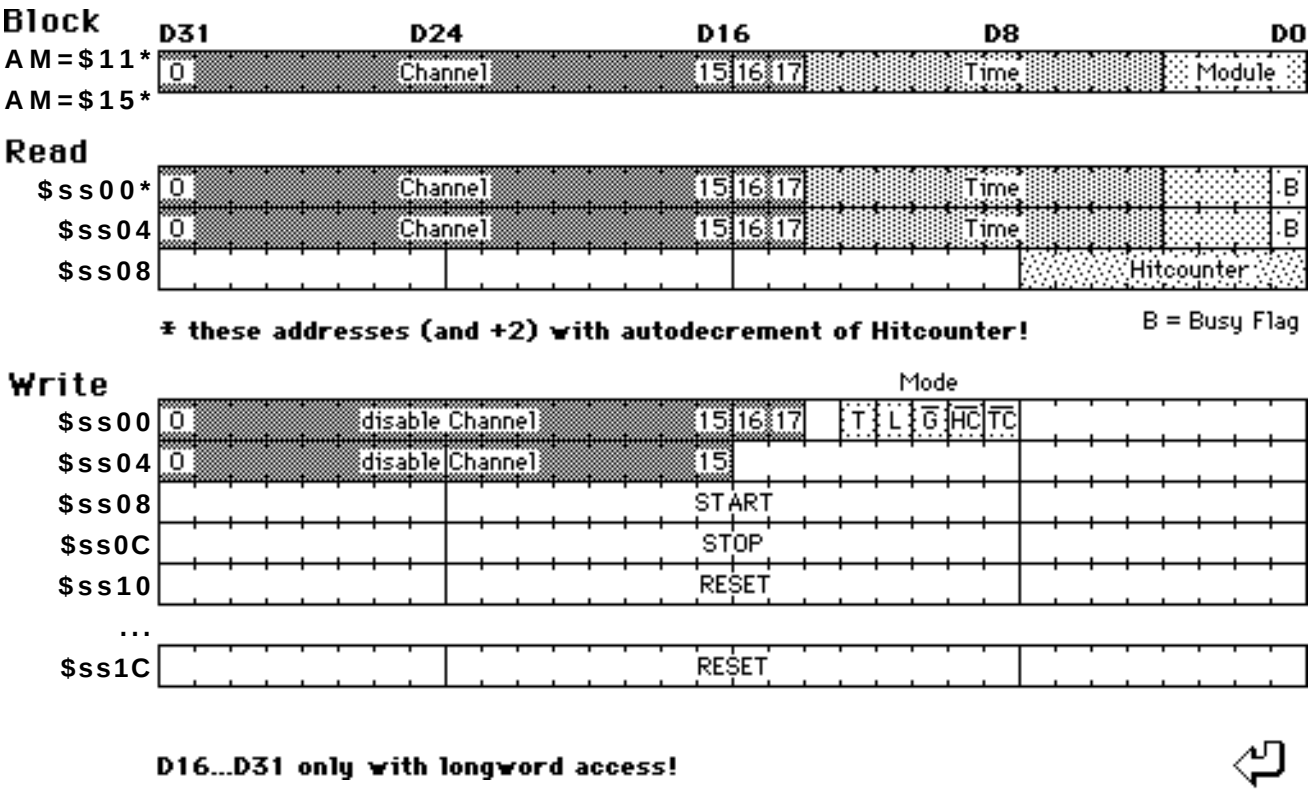
c) NOT TC-STOP + HC-STOP: The TDC stops only on HitCounter overrun.
This is a COMMON START mode where the TDC records everything until the memory is filled.
-High signal rates: only the first 255 hits (after start) are valid!
-Low signal rates: all n<255 hits are valid! The memory is also filled with TC overrun markers!
-No signals: the memory is only filled with TC overrun markers!

c) NOT TC-STOP + NOT HC-STOP: The TDC stops only on software RESET, STOP or ext. STOP/GATE or RESET.
This is the typical COMMON STOP mode where the TDC records everything until it will be stopped.
-High signal rates: only the last 255 hits (before stop) are valid!
-Low signal rates: only the last n<255 hits are valid! Also TC overrun markers!
-No signals: the memory is only filled with TC overrun markers!

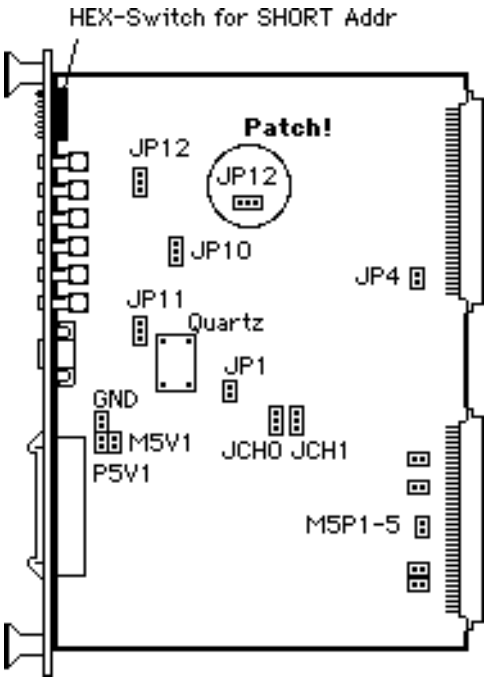
DL501 Functions

Function	Addr	Data	Remark
DL501Reset	w.SIO.$ss1x		reset HC, TC, flags; do Stop;
DL501Dec&Hit	r.SIO.$ss00	D31…D0	decrement HC & read HITSLICE
	(r.AM=$11)	D0	Busy flag
	(r.AM=$15)	D3…D1	Module Number (only 3 bits)
		D13…D4	TIME (10 bits)
		D31…D14	CHANNEL pattern (Ch0…Ch17)
DL501Hit	r.SIO.$ss04	D31…D0	read HITSLICE (no decrement!)
DL501HC	r.SIO.$ss08	D9…D0	read HITCOUNTER (HC)
DL501Start	w.SIO.$ss08		generate software START
DL501Stop	w.SIO.$ss0C		generate software STOP
DL501DisChannel	w.SIO.$ss04	D31…D16	disable CHANNELS (Ch0…Ch15)
DL501Mode	w.SIO.$ss00	D31…D14	disable CHANNELS (Ch0…Ch17)
		D8	(/TC) disable TimeCounterStop mode
		D9	(/HC) disable HitCounterStop mode
		D10	(/G) disable Gated mode (=Start/Stop mode)
	ss = SIO Addr	D11	(LM) enable LastModule mode
	w. = write	D12	(T) enable Trigger (Trigger only external)
	r. = read		
	x = don't care		

DL501 Memory Map



DL501 Jumper

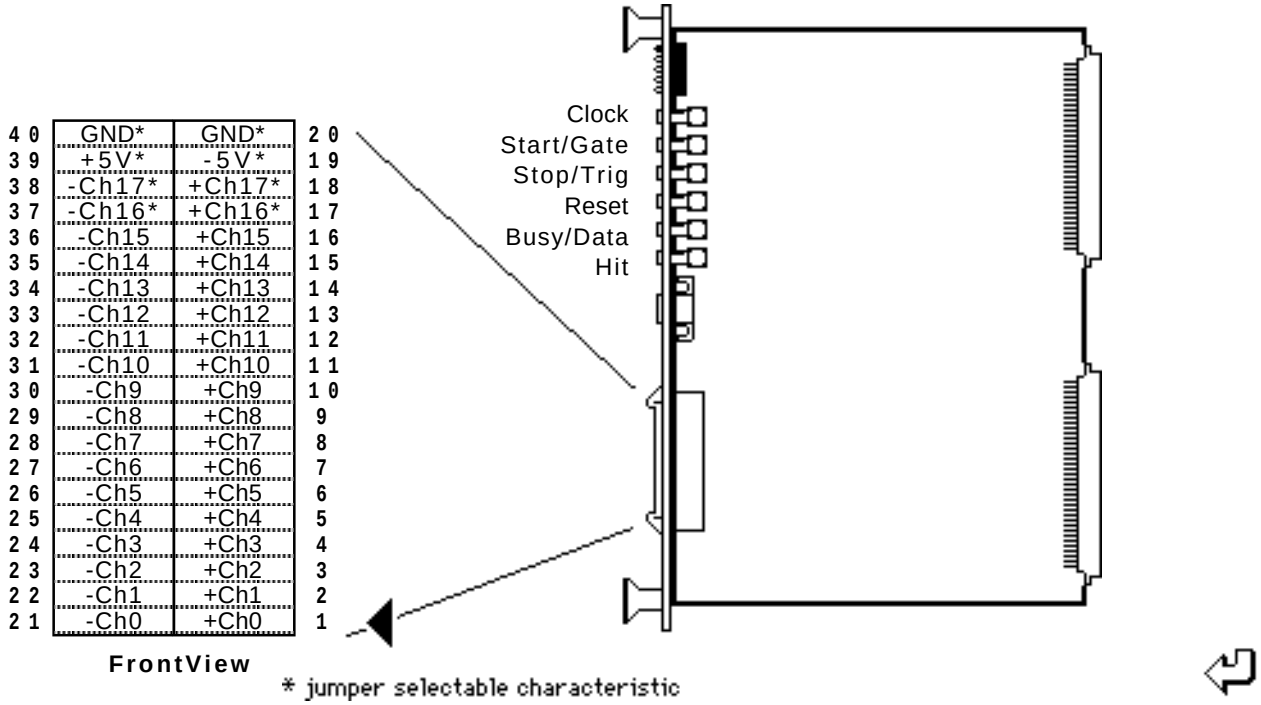


Jumper	Pos	Function
M5P1-5	closed*	-5.2V via P2 (VXI)
JP4	closed	BERR on VME-Bus
JP1	closed*	Auto Trigger
JP10	up	Busy/Data = Data
	down	Busy/Data = Busy
JP11	up	external Clock
	down	internal Clock
JP12	left	internal SetEmpty (HC=0)
(patched)	right	ext. SetEmpty (TimeMonitor)
P5V1	closed*	+5V on FrontConnector
M5V1	closed*	-5.2V on FrontConnector
GND	closed*	GND on FrontConnector
JCH0	up	Ch16 Edge
	down	Ch16 Status
JCH1	up	Ch17 Edge
	down	Ch17 Status

* prewired!

DL501 FrontConnector

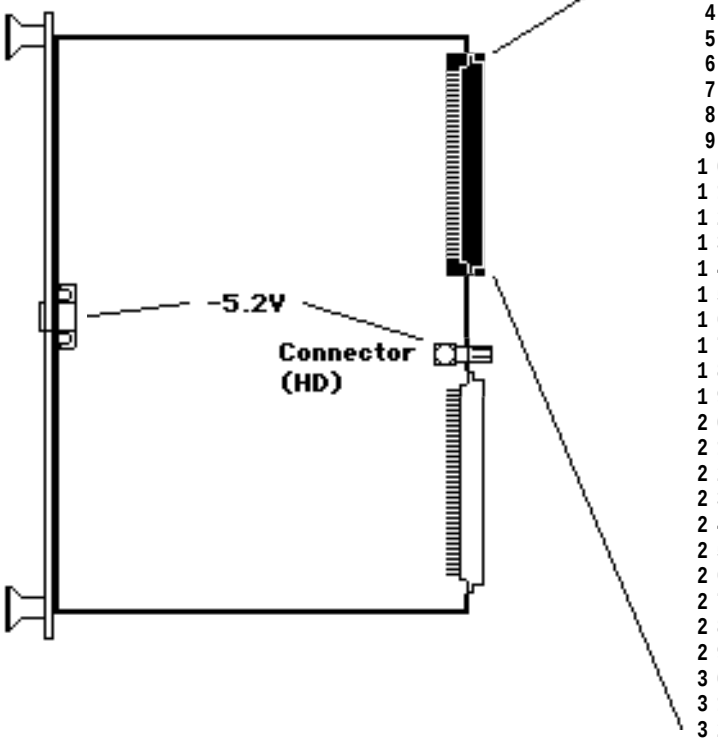
40	GND*	GND*	20
39	+5V*	-5V*	19
38	-Ch17*	+Ch17*	18
37	-Ch16*	+Ch16*	17
36	-Ch15	+Ch15	16
35	-Ch14	+Ch14	15
34	-Ch13	+Ch13	14
33	-Ch12	+Ch12	13
32	-Ch11	+Ch11	12
31	-Ch10	+Ch10	11
30	-Ch9	+Ch9	10
29	-Ch8	+Ch8	9
28	-Ch7	+Ch7	8
27	-Ch6	+Ch6	7
26	-Ch5	+Ch5	6
25	-Ch4	+Ch4	5
24	-Ch3	+Ch3	4
23	-Ch2	+Ch2	3
22	-Ch1	+Ch1	2
21	-Ch0	+Ch0	1



FrontView

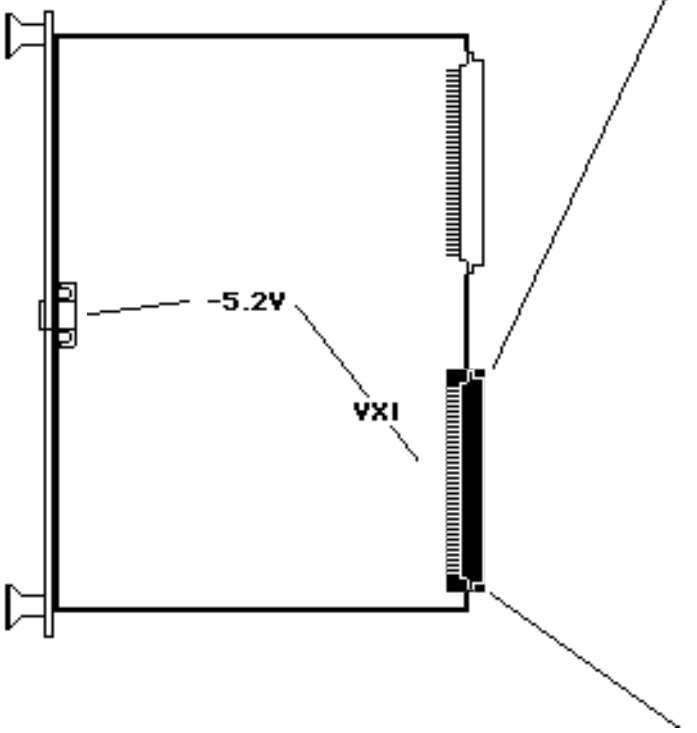
* jumper selectable characteristic

DL501 VMEConnector



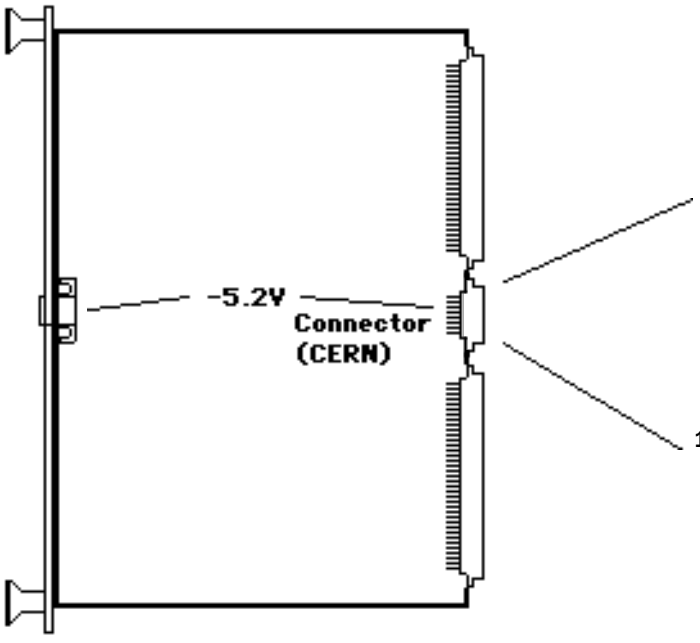
	a	b	c
1	D00	/BBSY	D08
2	D01	/BCLR	D09
3	D02	/ACF	D10
4	D03	/BGOI	D11
5	D04	/BG00	D12
6	D05	/BG1I	D13
7	D06	/BG1O	D14
8	D07	/BG2I	D15
9	GND	/BG2O	GND
10	SYSCLK	/BG3I	/SYSFAIL
11	GND	/BG3O	/BERR
12	/DS1	/BR0	/SYSR.
13	/DS0	/BR1	/LWRD
14	WRITE	/BR2	AM5
15	GND	/BR3	A23
16	DTACK	AM0	A22
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	SERC.	A17
22	/IACKO	SERD.	A16
23	AM4	GND	A15
24	A07	/IRQ7	A14
25	A06	/IRQ6	A13
26	A05	/IRQ5	A12
27	A04	/IRQ4	A11
28	AO3	/IRQ3	A10
29	A02	/IRQ2	A09
30	A01	/IRQ1	A08
31	-12V	+5VSB	+12V
32	+5V	+5V	+5V

DL501 VMX/VXIConnector



	a	b	c
1		+5V	
2	-2V	GND	
3		- - -	
4	GND	A24	-5.2V
5		A25	
6		A26	
7	-5.2V	A27	GND
8		A28	
9		A29	
10	GND	A30	GND
11		A31	
12		GND	
13	-5.2V	+5V	-2V
14		D16	
15		D17	
16	GND	D18	GND
17		D19	
18		D20	
19	-5.2V	D21	-5.2V
20		D22	
21		D23	
22	GND	GND	GND
23		D24	
24		D25	
25	+5V	D26	GND
26		D27	
27		D28	
28	GND	D29	GND
29		D30	
30		D31	GND
31	GND	GND	
32		+5V	

DL501 PowerConnector



	a	b	c
1	SN1	GND	SN2
2	SN3	GND	SN4
3	SN5	GND	GND
4	/CK	GND	CK
5	/SG	GND	SG
6	/CL	GND	CL
7	-2V	-2V	-2V
8	Res	CE	Res
9	-5V	-5V	-5V
10	-5V	-5V	-5V

CK = Clock
SG = Start/Stop Gate
CL = Clear
CE = Clean Earth
Res = reserved
SN = Slot Number
/ = negative logic